# Agilent N5106A PXB MIMO Receiver Tester
# Security Features

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## Notice

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# Purpose of this Document

This document describes instrument security features and the steps to declassify an instrument through memory removal. For additional information, please refer to: http://www.agilent.com/find/security

**NOTE** Be sure that all information stored by the user (such as traces, status, etc.) in the instrument that needs to be saved is properly backed up before attempting to clear any of the instrument memory. Agilent Technologies cannot be held responsible for any lost files or data resulting from the clearing of memory. Be sure to read this document entirely before proceeding with any file deletion or memory clearing.

## Products Covered by this Document

**Model:** N5106A

**Product Name:** PXB MIMO Receiver Tester

"Instrument Memory Locations" on page 5 provides a detailed summary of each of the memory locations contained with the PXB.

## Terms and Definitions

*Clearing* Clearing is the process of eradicating the data on media before reusing the media so that the data can no longer be retrieved using the standard interfaces on the instrument. Clearing is typically used when the instrument is to remain in an environment with an acceptable level of protection.

*Sanitization* Sanitization is the process of removing or eradicating stored data so that the data cannot be recovered using any known technology. Instrument sanitization is typically required when an instrument is moved from a controlled area to a non-controlled area such as when it is returned to the factory for calibration (the instrument is declassified). Agilent memory sanitization procedures are designed for customers who need to meet the requirements specified by the U.S. Defense Security Service (DSS). These requirements are outlined in the "Clearing and Sanitization Matrix" issued by the Cognizant Security Agency (CSA) and referenced in National Industrial Security Program Operating Manual (NISPOM) DoD 5220.22M ISL 01L-1 section 8-301.

*Security erase* Security erase is a term that is used to refer to either the clearing or sanitization features of Agilent instruments.

*Instrument declassification* A term that refers to procedures that must be undertaken before an instrument can be removed from a controlled area such as is the case when the instrument is returned for calibration. Declassification procedures will include memory sanitization and or memory removal. Agilent declassification procedures are designed to meet the requirements specified by the DSS NISPOM security document (DoD 5220.22M chapter 8).

# Instrument Memory Locations

## Instrument Non-Volatile Memory

This section contains information on the types of non-volatile memory available in your instrument. It explains the size of memory, how it is used, its location, and the sanitization procedure.

**Table 1 Summary of PXB Non-Volatile Memory**

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| Board ID Memory (EEPROM) 256 Kb | No | Yes | Header EEPROM used to identify assembly and revision. | Programmed before board assembly. | N5105-63002 Interconnect Board (U300) N5105-80004 | None |
| License Storage Memory (EEPROM) 512 Kb | No | Yes | Contains instrument serial number and license keys for instrument applications. | Programmed before board assembly, when new licenses are installed, or by factory/service center calibration software. | N5105-63003 Midplane Board (U32) N5105-80016 | None |
| Control Logic Memory (CPLD) 32 macrocells | No | Yes | Contains configuration information for PCI Express switches and master/slave functionality. | Programmed before board assembly or by factory/service center calibration software. | N5105-63003 Midplane Board (U50) N5105-80011 | None |
| PCIe SW1 Int Config Memory (EEPROM) 256 Kb | No | Yes | Contains configuration information for PCI Express switch 1 when using internal host. | Programmed before board assembly. May be reprogrammed with switch manuacturer software. | N5105-63003 Midplane Board (U57) N5105-80013 | None |
| PCIe SW1 Ext Config Memory (EEPROM) 256 Kb | No | Yes | Contains configuration information for PCI Express switch 1 when using external host. | Programmed before board assembly. May be reprogrammed with switch manuacturer software. | N5105-63003 Midplane Board (U33) N5105-80002 | None |
| PCIe SW2 Int Config Memory (EEPROM) 256 Kb | No | Yes | Contains configuration information for PCI Express switch 2 when using internal host. | Programmed before board assembly. May be reprogrammed with switch manuacturer software. | N5105-63003 Midplane Board (U34) N5105-80003 | None |
| IO Expander (EEPROM) 64 bytes | Yes | Yes | Contains configuration for master versus slave operation. | Programmed via user interface. | N5105-63003 Midplane Board (U49) | None |
| (FLASH) 8 Mb | No | Yes | Contains configuration information for PCI Express FPGA. | Programmed before board assembly. Field upgrade by service only. | N5105-63004 Baseband Board (U52) N5105-80005 Contains no user data | None |
| (FLASH) 8 Mb | No | Yes | Contains configuration information for PCI Express FPGA. | Programmed before board assembly. Field upgrade by service only. | N5105-63004 Baseband Board (U53) N5105-80006 Contains no user data | None |
| Board ID Memory (EEPROM) 256 Kb | No | Yes | Header EEPROM used to identify assembly and revision. | Programmed before board assembly. | N5105-63005 DRAM Board (U301) Contains no user data | None |

## Table 1 Summary of PXB Non-Volatile Memory

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| EEPOT (EEMEM) 14 bytes | No | Yes | Stores optimum varactor bias for 100 MHz crystal oscillator. | Programmed during board test and by service center. | N5105-63006 Clock Board (U202) Contains no user data | None |
| (EEPROM) 256 Kb | No | Yes | Header EEPROM used to identify assembly and revision. | Programmed prior to assembly. | N5105-63006 Clock Board (U601) N5105-80015 Contains no user data | None |
| FLASH 4 Mb | | | Contains programming information for FPGA1 on Clock Board. | Programmed prior to assembly. May be reprogrammed in the field by firmware upgrades. | N5105-63006 Clock Board (U1219) N5105-80001 Contains no user data | None |
| CPLD XC9572XL 72 macrocells | No | Yes | Contains fixed digital logic associated with front-panel keyboard operation. | Programmed prior to assembly. May be reprogrammed by the service center. | N5105-63008 Front Panel Assy (U24) W1312-80018 Contains no user data | None |
| PIC µController PIC18LF4455 24 KB FLASH 256 bytes EEPROM | No | Yes | Contains program code for front-panel microcontroller. Transmits key presses to system processor. | Programmed prior to assembly. May be reprogrammed during a firmware upgrade. | N5105-63008 Front Panel Assy (U17) W1312-80015 Contains no user data | None |
| Display ID (EEPROM) 2 Kb | No | Yes | Extended display identification data is a standard data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory preset timings, frequency range limits, and character strings for the monitor name and serial number. | Programmed prior to assembly. | N5105-63008 Front Panel Assy (U26) E6601-87009 Contains no user data | None |
| EEPROM 256 Kb | No | Yes | Header EEPROM used to identify assembly and revision. | Programmed prior to assembly. | N5105-63009 IO Board (U5) N5105-80008 Contains no user data | None |
| EEPROM | Yes | Yes | Contains configuration information for touchscreen performance and calibration. | Programmed prior to assembly and is reprogrammed by touchscreen application. | N5105-60018 Touchscreen Controller Contains no user data | None |
| Main Memory (Hard Disc Drive) 160 GB | Yes | Yes | Contains operating system, instrument software, factory calibration data, recovery image, user instrument states, user data files, user trace data and any user-installed software. | Programmed before assembly, by factory/ service center calibration software, or by software upgrade installation. Also via instrument software operations and by user. | W1312-60057 Hardware platform processor Contains user data | None |
| CPU BIOS (CMOS NVRAM) 256 bytes | No | Yes | Contains default BIOS settings to use when booting the hardware platform processor. | Programmed by factory and settings can be toggled by user. | W1312-60057 Hardware platform processor battery backed-up to maintain calendar time. Contains no user data. | None |

**Table 1 Summary of PXB Non-Volatile Memory**

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| | No | Yes | Contains operating code for power supply mainframe. | Programmed by Astec. | Astec Power Supply Mainframe<br>Contains no user data. | None |
| | No | Yes | Contains operating code for +12 Vdc power supply module. | Programmed by Astec. | Astec Power Supply +12 Vdc Module<br>Contains no user data. | None |
| | No | Yes | Contains operating code for +12 Vdc power supply module. | Programmed by Astec. | Astec Power Supply +12 Vdc Module<br>Contains no user data. | None |
| | No | Yes | Contains operating code for +5 Vdc and +16.5 Vdc power supply module. | Programmed by Astec. | Astec Power Supply +16.5 Vdc/+5.1 Vdc Module<br>Contains no user data. | None |
| | No | Yes | Contains operating code for +3.3 Vdc power supply module. | Programmed by Astec. | Astec Power Supply +3.3 Vdc Module<br>Contains no user data. | None |

## Instrument Volatile Memory

The PXB MIMO Receiver Tester also contains volatile memories. The volatile memories are not battery backed-up. They do not retain any information when AC power is removed. Removing power from these memories meets the memory sanitization requirement in the “Clearing and Sanitization Matrix” referenced in DoD 5220.22M 1SL 01L-1 section 8-301 as current on 06/27/2005.

**Table 2 Summary of PXB Volatile Memory**

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| FPGA<br>XC4VFX60<br>56,880 cells<br>4,176 Kb RAM | Yes | No | Channel 1 switch matrix for data routing. | Written to during application program execution. | N5105-60002 Interconnect Board (U1)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VFX60<br>56,880 cells<br>4,176 Kb RAM | Yes | No | Channel 2 switch matrix for data routing. | Written to during application program execution. | N5105-60002 Interconnect Board (U2)<br>Contains no user data | Turn off instrument power |
| USB Controller (RAM)<br>16 KB | Yes | No | Microcontroller for the Interconnect Board. Software communicates with this controller through USB interface. | Written to during application program execution. | N5105-60002 Interconnect Board (U302)<br>Contains no user data | Turn off instrument power |
| DSP<br>ADSP-TS201S (DRAM)<br>24 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U35)<br>Contains no user data | Turn off instrument power |
| DSP<br>ADSP-TS201S (DRAM)<br>24 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U36)<br>Contains no user data | Turn off instrument power |
| Baseband signal processing ASIC control registers<br>192 bytes | Yes | No | Computation coefficient storage. | Written to during application program execution. | N5105-60104 Baseband Board (U37)<br>Contains no user data | Turn off instrument power |
| Baseband signal processing ASIC control registerss<br>192 bytes | Yes | No | Computation coefficient storage. | Written to during application program execution. | N5105-60104 Baseband Board (U38)<br>Contains no user data | Turn off instrument power |
| SRAM<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U54)<br>Contains no user data | Turn off instrument power |
| SRAM<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U55)<br>Contains no user data | Turn off instrument power |
| SRAM<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U56)<br>Contains no user data | Turn off instrument power |
| (SRAM)<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U57)<br>Contains no user data | Turn off instrument power |
| (SRAM)<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U58)<br>Contains no user data | Turn off instrument power |

**Table 2 Summary of PXB Volatile Memory**

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| (SRAM)<br>18 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U59)<br>Contains no user data | Turn off instrument power |
| (DRAM)<br>128 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U60)<br>Contains no user data | Turn off instrument power |
| (DRAM)<br>128 Mb | Yes | No | Computation data storage. | Written to during application program execution. | N5105-60104 Baseband Board (U61)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC3S1200<br>19,512 cells<br>RAM<br>136 Kb distributed<br>504 Kb block | Yes | No | Logic function configuration data. | Written to during application program execution. | N5105-60104 Baseband Board (U68)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VSX55<br>55,296 cells<br>5,760 Kb RAM | Yes | No | Logic function configuration data. | Written to during application program execution. | N5105-60104 Baseband Board (U69)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VFX60<br>56,880 cells<br>4,176 Kb RAM | Yes | No | Logic function configuration data. | Written to during application program execution. | N5105-60104 Baseband Board (U79)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VSX55<br>55,296 cells<br>5,760 Kb RAM | Yes | No | Logic function configuration data. | Written to during application program execution. | N5105-60104 Baseband Board (U99)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VLX25<br>24,192 cells<br>1,296 Kb RAM | Yes | No | Data routing and memory controller. | Written to during application program execution. | DRAM Board (U1)<br>(Part of N5105-60104 Baseband Board)<br>Contains no user data | Turn off instrument power |
| (SRAM)<br>18 Mb | Yes | No | User waveform sequencing. | Written to during application program execution. | DRAM Board (U300)<br>(Part of N5105-60104 Baseband Board)<br>Contains no user data | Turn off instrument power |
| (DRAM)<br>1 Gb | Yes | No | User waveform storage. | Written to during application program execution. | DRAM Board<br>(Part of N5105-60104 Baseband Board)<br>Contains user signal data | Turn off instrument power |
| (DRAM)<br>1 Gb | Yes | No | User waveform storage. | Written to during application program execution. | DRAM Board<br>(Part of N5105-60104 Baseband Board)<br>Contains user signal data | Turn off instrument power |
| (DRAM)<br>1 Gb | Yes | No | User waveform storage. | Written to during application program execution. | DRAM Board<br>(Part of N5105-60104 Baseband Board)<br>Contains user signal data | Turn off instrument power |

**Table 2 Summary of PXB Volatile Memory**

| Memory Type and Size | Writable During Normal Operation? | Data Retained When Powered Off? | Purpose/Contents | Data Input Method | Location in Instrument and Remarks | Sanitization Procedure |
|---|---|---|---|---|---|---|
| (DRAM)<br>1 Gb | Yes | No | User waveform storage. | Written to during application program execution. | DRAM Board<br>(Part of N5105-60104 Baseband Board)<br>Contains user signal data | Turn off instrument power |
| FPGA<br>XC3S500<br>10,476 cells<br>RAM<br>73 Kb distributed<br>360 Kb block | Yes | No | Controls the main phase lock loop for the system, and controls clock routing functionality of the PXB. | Written to during application program execution. | N5105-60006<br>Clock Board (U400)<br>Contains no user data | Turn off instrument power |
| USB Controller<br>(RAM)<br>16 KB | Yes | No | Microcontroller for the Clock Board. Software communicates with this controller through USB interface. | Written to during application program execution. | N5105-60006<br>Clock Board (U600)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC3S400<br>8,064 cells<br>360 Kb RAM | Yes | No | Controls trigger and marker functionality. | Written to during application program execution. | N5105-60006<br>Clock Board (U1000)<br>Contains no user data | Turn off instrument power |
| PIC µController<br>PIC18LF4455<br>2 KB SRAM | Yes | No | Temporary storage used by front panel keyboard controller. | Written to by normal keyboard use. Not accessible by user. | N5105-60008<br>Front Panel Assy (U17)<br>Contains no user data | Turn off instrument power |
| USB Controller<br>(RAM)<br>16 KB | Yes | No | Microcontroller for the IO Board. Software communicates with this controller through USB interface. | Written to during application program execution. | N5105-60009<br>IO Board (U16)<br>Contains no user data | Turn off instrument power |
| Baseband signal processing ASIC control registers<br>192 bytes | Yes | No | Registers which dictate Channel 1 baseband signal processing ASIC configuration. | Written to during application program execution. | N5105-60009<br>IO Board (U15)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VLX25<br>24,192 cells<br>1,296 Kb RAM | Yes | No | Controls IO functionality for Channel 1. Sets up the digital bus interface ports, communicates with the baseband signal processing ASIC, and controls analog output. | Written to during application program execution. | N5105-60009<br>IO Board (U13)<br>Contains no user data | Turn off instrument power |
| Baseband signal processing ASIC control registers<br>192 bytes | Yes | No | Registers which dictate Channel 2 baseband signal processing ASIC configuration. | Written to during application program execution. | N5105-60009<br>IO Board (U18)<br>Contains no user data | Turn off instrument power |
| FPGA<br>XC4VLX25<br>24,192 cells<br>1,296 Kb RAM | Yes | No | Controls the IO functionality for Channel 2. Sets up the digital bus interface ports, communicates with the baseband signal processing ASIC, and controls analog output. | Written to during application program execution. | N5105-60009<br>IO Board (U17)<br>Contains no user data | Turn off instrument power |
| (DRAM)<br>4 Gb | Yes | No | Main dynamic RAM memory for Intel processor. Contains working copies of operating system, instrument firmware personalities, calibration data, and measurement data. | Written to by firmware operations and by the user. | W1312-60057<br>Hardware platform processor<br>Contains user data. This memory is not battery backed-up or connected to standby power. | Turn off instrument power |

# Using the PXB in a Controlled Area

The only non-volatile user memory storage location in the PXB instrument is the A14 hard drive assembly. The remainder of the user-accessible PXB memory storage is in volatile memory which is deleted/erased when the power is removed from the instrument.

The PXB does not have an erasure and sanitization procedure to cleanse the A14 hard drive assembly.

When a PXB instrument is used within a controlled area and the need arises to remove it from that controlled area, the security strategy is to remove the A14 hard drive assembly from the PXB and leave the removed hard drive in the controlled area.

## Before Placing the PXB in a Controlled Area

Before moving the PXB into a controlled area, ensure that the latest firmware revision is installed on the instrument. Refer to the PXB firmware upgrade guide for complete instructions. This document is available at:

http://www.agilent.com/find/upgradeassistant

This is the same web page where you can download the latest firmware revision.

## Removing the PXB from a Controlled Area

If you need to remove the PXB from a controlled area, you will need to remove the A14 hard drive assembly from the instrument to protect sensitive information from leaving the controlled area. Use the following procedure:

1. While the instrument is located inside the controlled area, remove the A13 CPU assembly from the PXB.

   Refer to the PXB Guided Service and Support documentation (most current version is available on the Technical Support tab of http://www.agilent.com/find/pxb) for instructions.

2. Remove the A14 hard drive assembly from the CPU assembly.
3. On the hard drive assembly, mark the PXB model number, the serial number, and that it is for the controlled area. Store the hard drive assembly in the controlled area for safe keeping until the PXB is returned to this area.
4. Reinstall the A13 CPU assembly (without the hard drive assembly) into PXB and remove the instrument from the controlled area.

### To Return the PXB to Agilent for Repair

The PXB can now be sent to the Agilent service center for repair without the PXB's A14 hard drive assembly installed.

**NOTE** Be sure to note on the documents being shipped with the PXB to the Agilent repair center that the A14 hard drive has been removed to protect your sensitive information.

- If the PXB is under warranty, the A14 hard drive will be replaced without charge.
- If the PXB is out of warranty, the A14 hard drive will be replaced and you will be billed for this new assembly as part of the repair.

**NOTE** In both cases, the PXB will be returned with the A14 hard drive assembly that was installed by Agilent repair personnel. After receiving the PXB back from the repair facility, refer to "Returning the PXB to the Controlled Area" on page 12 before placing your PXB back in a controlled area.

### To Use or Repair the PXB in the Non-controlled Area

After the PXB has left the controlled area, to use or repair it in a non-controlled area, you will need a backup imaged hard drive to install into the CPU.

1. Before it is installed, mark the PXB model number and serial number on the hard drive. It would also be good to note on it that it is for the non-controlled area.
2. Remove the CPU assembly from the PXB.
3. Install the hard drive into CPU assembly and reinstall the CPU assembly into the PXB.

## Returning the PXB to the Controlled Area

This section provides detailed steps required to return your PXB to a controlled area after the PXB was repaired or used ou the controlled area. Follow the applicable procedure listed below:

- If you removed the PXB from the controlled area to use it in a non-controlled area, refer to "After Using the PXB in the Non-Controlled Area" on page 12.
- If you removed the PXB from the controlled area to send it for repair, refer to "After Repairing the PXB" on page 13.

**NOTE** For instructions on installing and removing the A13 CPU and the A14 hard drive assemblies, refer to the PXB Guided Service and Support documentation which is available by selecting the Technical Support tab on: http://www.agilent.com/find/pxb

### After Using the PXB in the Non-Controlled Area

1. While the instrument is still in the non-controlled area, remove the A13 CPU assembly from the PXB.
2. Remove the A14 hard drive assembly from the CPU assembly.
3. If the hard drive assembly is not labeled, mark the PXB model number and serial number and that the hard drive assembly is designated to be used in the non-controlled area. This hard drive can be kept in the non-controlled area for use there. Store the hard drive assembly in an ESD-safe storage container.
4. Reinstall the A13 CPU assembly (without the hard drive assembly) into PXB and move the instrument

to the controlled area.

5. Once in the controlled area, remove the A13 CPU assembly from the PXB.
6. Install the A14 hard drive assembly into the A13 CPU assembly.

   This is the hard drive assembly that was removed from the PXB and stored in your controlled area before the PXB was removed from the controlled area.
7. Reinstall the CPU with the hard drive into the PXB. The PXB is now ready for use in the controlled area.

### After Repairing the PXB

1. While the instrument is still in the non-controlled area, read the repair documentation to identify the cause of repair.
2. If the repair documentation indicates that the A14 hard drive assembly:
   - Was the cause of the repair, move the PXB into the controlled area. The PXB is now ready for use in the controlled area.
   - Was not the cause of the repair, the returned hard drive should not be removed from the PXB and kept in non-controlled area for use outside the controlled area. Follow these steps:

     a. Remove the A13 CPU assembly from the PXB and remove the A14 hard drive assembly from the CPU assembly.

     b. On the hard drive assembly that was just removed, mark the PXB model number and serial number and that it will be used in the non-controlled area. Store the hard drive assembly in an ESD-safe storage container in the non-controlled area.

     c. Reinstall the A13 CPU assembly (without the hard drive assembly) into PXB and move the instrument to the controlled area.

     d. Once in the controlled area, remove the A13 CPU assembly from the PXB.

     e. Install the A14 hard drive assembly for this PXB serial number (kept in your controlled area while the PXB was being repaired) into the A13 CPU assembly.

     f. Reinstall the CPU with the hard drive into the PXB. The PXB is now ready for use in the controlled area.

# Contacting Agilent Sales and Service Offices

Assistance with test and measurements needs and information on finding a local Agilent office is available on the Internet at:

http://www.agilent.com/find/assist

If you do not have access to the Internet, please contact your field engineer.

**NOTE** In any correspondence or telephone conversation, refer to the instrument by its model number and full serial number. With this information, the Agilent representative can determine whether your unit is still within its warranty period.